Master of Technology in **Embedded Systems**

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology Jaipur

Subject Code	Course Title	Category	Type	Credits Total	L T P
Semester 1 (Taught Courses-6)					
ECT701	Data Structures & Algorithms	Core	Theory	3	3-0-0
ECT702	Advanced Microcomputer Systems & Interfacing	Core	Theory	3	3-0-0
ECT912[§]	Reduced order Modeling, Optimization & Machine intelligence	Core	Theory	2	2-0-0
ECP709	Hardware Systems Lab	Core	Lab	1.5	0-0-3
ECP711	Software Systems lab	Core	Lab	1.5	0-0-3
	(Elective Courses)"				
	Program Elective (PE-1)	Elective	Theory	3	
	Program Elective (PE-2)	Elective	Theory	3	
	Total Semester Credits			**11+6=17**	
Semester 2 (Taught courses- 5)					
ECT704	Computer vision	Core	Theory	3	3-0-0
ECP712	System Design Lab	Core	Lab	3	0-0-6
ECP900	Technical Documentation	Core	Theory	1	0-0-2
ECD656	[Minor Project (Research Project)][†]				
	(Elective Courses)"				
	Program Electives (PE-3)	Elective	Theory	3	
	Program Electives (PE-4)	Elective	Theory	3	
	Program Electives (PE-5)	Elective	Theory	3	
	MOOC[‡]	Optional	Blended		
	Total Semester Credits			**7+9=16**	
	List of Elective Courses				
ECT616	Computer Arithmetic & Micro-architecture Design		Theory	3	3-0-0
ECT618	Graph Algorithms & Combinatorial optimization		Theory	3	3-0-0
ECT622	System Level Design & Modeling		Theory	3	3-0-0
ECT624	VLSI Testing & Testability		Theory	3	3-0-0
ECT626	Formal Verification of Digital Hardware & Embedded Software		Theory	3	3-0-0
ECT628	Memory Design & Testing		Theory	3	3-0-0
ECT630	Advance Computer Architecture		Theory	3	3-0-0
ECT631	Digital System Design & FPGAs		Theory	3	3-0-0
ECT632	Embedded SoC Design		Theory	3	3-0-0
ECT634	Micro-& Nano-electro-mechanical Systems (MEMS & NEMS)		Theory	3	3-0-0
ECT638	Design of Asynchronous Sequential Circuits		Theory	3	3-0-0
ECT642	FPGA's Physical Design		Theory	3	3-0-0
ECT648	Languages for (i) Hardware Description, (ii) Scripting and (iii) Simulation/verification; (alternately, 1-credit each for these parts)		Theory	3	3-0-0
ECT652	RF MEMS		Theory	3	3-0-0
ECT654	RF Integrated Circuits		Theory	3	3-0-0
ECT656	Adaptive Signal Processing		Theory	3	3-0-0
ECT657	VLSI Signal Processing Architectures		Theory	3	3-0-0
ECT662	Advanced Digital Signal & Image Processing		Theory	3	3-0-0
ECT690	Wireless Sensor Networks		Theory	3	3-0-0
ECT703	CAD Algorithms for Synthesis of VLSI Systems		Theory	3	3-0-0
ECT706	Advanced Embedded software design		Theory	3	3-0-0

[†] *The Minor/Research project is placed in 3rd Semester only. However, for students desirous of INTENRSHIP in 3rd Semester, this Minor project (Research Project) would have to be completed in 2nd Semester.*

[‡] *MOOC course is OPTIONAL and over and above the scheme credits, i.e. NOT mandatory and not counted towards minimum credits required for degree*

Kuldeep Singh Chitrakant Sahu Tarun Varma Lava Bhargava Vineet Sahula

Master of Technology in **Embedded Systems**

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology Jaipur

Subject Code	Course Title	Category	Type	Credits Total	L T P
ECT733	Pattern Analysis & Machine Intelligence		Theory	3	3-0-0
ECT734	Internet of Things (IoE) & IIoT		Theory	3	3-0-0
ECT735	Probabilistic Machine Learning & AI		Theory	3	3-0-0
ECT736	Medical Engineering & Systems		Theory	3	3-0-0
ECT740	Embedded Intelligent Systems		Theory	3	3-0-0
ECT741	Quantum Computing		Theory	3	3-0-0
			Theory	3	3-0-0
CPT602	Parallel & Distributed Systems		Theory	3	3-0-0
ECT912	Modeling, Optimization & Transforms		Theory	3	3-0-0
ECT914	Modeling & Simulation for Communication Engineering		Theory	2	2-0-0
ECT992	Mathematical Methods & Techniques for ECE Technologists-II		Theory	2	2-0-0
			Theory	3	3-0-0
	Fractional credit courses				
ECT761	Special Modules in Embedded Systems Design-I		Theory	1	1-0-0
ECT762	Special Modules in Embedded Systems Design-II		Theory	1	1-0-0
ECT763	Special Modules in Embedded Systems Design-III		Theory	1	1-0-0
ECT764	Special Modules in Embedded Systems Design-IV		Theory	1	1-0-0
ECT648A	Hardware Description Language		Theory	1	1-0-0
ECT648B	Scripting Language		Theory	1	1-0-0
ECT648C	Language to support Simulation/verification		Theory	1	1-0-0
			Theory	1	1-0-0
	Semester 3				
	Minor Project (Research Project)[$]	Core	Research project	4	0-0-8
ECD659	Dissertation	Core	Dissertation	6	0 0 12
	Total Semester Credits			**4+6=10**	
	Semester 4				
ECD660	Dissertation	Core	Dissertation	12	(0 0 24)
	Total Semester Credits			**12**	
	Total minimum Credits of all semesters (a student might cover more credits > 55)			**55**	

Sem I	Taught courses + Lab	17
Sem II	Taught courses	16
Sem III	Minor Project (Research Project), Dissertation	4+6=10
Sem IV	Dissertation	12
	Total	**55**

Programme core	18
Programme electives	15
Open elective	00
Minor Project (Research project)	04
Dissertation	18
Total	**55**

[$] *Only one course out of ECT910/ECT992, or ECT912/ECT914*

** *The students may opt for any course from MTech (Embedded Systems) or MTech (VLSI)*

Kuldeep Singh Chitrakant Sahu Tarun Varma Lava Bhargava Vineet Sahula

Master of Technology in **Embedded Systems**

Department of Electronics & Communication Engineering

Malaviya National Institute of Technology Jaipur

Core courses

Program: M Tech in Embedded Systems	**Department: Electronics & Communication Engineering**
Course Code: ECT631	**Course Name: Digital System Design & FPGAs**
Credit: 3	**L-T-P: 3-0-0**
Pre-requisites: None	
Objectives:	
COURSE DURATION: 12/13/14 weeks excluding examinations	

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components.

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

COURSE CONTENTS:

Unit-1: Sequential Logic Design-Introduction, Basic bistable Memory Devices, additional bistable devices, reduced characteristics and excitation table for bistable devices.

Unit-2: Synchronous Sequential Logic Circuit Design- Introduction, Moore, Mealy and Mixed type Synchronous State Machines. Synchronous sequential design of Moore, Mealy machines,

Unit-3: Asynchronous Sequential Logic Circuit Design- Introduction, analysis and synthesis of asynchronous State Machines. Hazards

Unit-4: Algorithmic State Machine- An Algorithm with inputs, digital solution, Implementation of traffic light controller, ASM charts, Design Procedure for ASMs.

Unit-5: Data path and Control design.

Unit-6: Introduction to FPGA: Basics of PLD, FPGA Design Tool Flow, Basic blocks of FPGA, State of art architectures of FPGA, Applications of FPGA; FPGA mapping of combinational & sequential designs

Course Outcomes:

CO1. To be able to apply the basic design principles of sequential logic systems. (Cognitive- Applying)

CO2. To understand the design concepts of synchronous and asynchronous state machines in Moore and Mealy architectures. (Cognitive- understanding)

CO3. To analyze & design data path, control path design and various programmable devices (Skills- Create)

CO4. To be able to implement a digital system using HDLs(Skills-Evaluate)

Text books:

1. Digital System Design, Ercegovac, Wiley.
2. Richard S. Sandige, *Modern Digital Design*, McGraw-Hill, 1990.
3. Zvi Kohavi, Switching and Finite Automata Theory, Tata McGraw-Hill.
4. Navabi. Analysis and modeling of digital systems. McGraw Hill, 1998.
5. Perry. Modeling with VHDL. McGraw Hill, 1994.
6. Navabi. Verilog Digital Design. McGraw Hill, 2007.
7. Fundamentals of Digital Logic with Verilog Design, Stephen Brown and Zvonko Vranesic, McGraw Hill, 2002.

References:

Online/E resources

1.

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT701	Course Name: Data Structure & Algorithms
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course: None	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Introduction to data structures. Static and dynamic aspects of memory allocation. Recursion and its applications. Introduction to complexity analysis, measure and representation.

Unit-2: Algorithms for searching and Sorting. Non-recursive and recursive implementation of searching. Non-recursive and recursive sorting algorithms.

Unit-3: Creation and manipulation of data structures: arrays, stacks, queues and linked lists with static and dynamic memory allocation. Applications.

Unit-3: Creation, manipulation and analysis of trees. Binary search tree algorithms.

Unit-3: Graph problems: Shortest path implementation. Introduction to Max Flow-Min Cut and travelling salesman problem.

Unit-3: Introduction to height balanced trees: AVL and B Trees.

Course Outcomes:

CO1. To impart the basic concepts of data structures and algorithms.
CO2. To understand concepts about searching and sorting techniques.
CO3. To understand basic concepts about stacks, queues, lists, trees, and graphs.
CO4. To understanding about writing algorithms and step by step approach in solving problems with the help of fundamental data structures.

Textbooks:

1. Rivest, Cormen, Introduction to Algorithms, MIT Press
2. Horowitz and Sahni: Data Structure in C++ , Glagotia
3. Ellis Horowitz, Sartaj Sahni, Fundamentals of Data Structures
4. Aaron M. Tenenbaum, Y. Langsam, Moshe J. Augenstein, Data Structures Using C

References:

Online/E resources

1.

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT702	Course Name: Advanced Microcomputer Systems & Interfacing
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Introduction; Processor-processor (Intel/ARM) and micro controller (Intel/ARM), assembly language programming,

Unit-2: Interfacing methods-protocols, synchronization, parallel I/O, serial I/O, Memory interfacing, Digital/Analog interfacing, high speed I/O interfacing, data acquisition systems, CAN, I2C, USB, ESSI (Enhanced Synchronous Serial Interface) protocols; General Purpose Input/Output (GPIO)

Unit-3: Interrupt Synchronization & Timing generation- Features of interrupts, interrupt vectors & priority, polling, priority algorithms; frequency measurement, frequency and period conversion.

Unit-4: Miscellaneous- Serial and parallel port interfaces; State machine & concurrent process models.

Unit-5: System examples- camera etc; Debugging: JTAG, ISP, BDM Port, BITP, and DB9 ports.

Course outcomes:

CO1. To Understand the 16,32,64-bit processors ISA (CISC and RISC)
CO2. To understand the language and use of micro controller (ARM/Atmega 328)
CO3. To understand different I/O interface protocols and write programs for ARM interfaces
CO4. To understand memory and different transducers and interfacing
CO5. To write assembly programmes interfacing and design issues of embedded system(analytically and design issues)

Textbooks:

1. Jonathan W. Valvano, Embedded Microcomputer Systems: Real-Time Interfacing, Brookes/Cole, Pacific Grove, 2000.
2. Douglas V. Hall , Microprocessors and interfacing, McGraw Hills,
3. K.Ayala, The 8051 Microcontroller, Thompsons, Mazidi,Naimi, Naimi , avr microcontroller and embedded system, pearsons.
4. David A. Patterson and John L. Hennessy, Computer Organization and design ARM ed.,Morgan Kaufmann,
5. F. Vahid & T. Givargis, Embedded System Design, Wiley.
6. Wolf, W., Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufmann, San Francisco, 2001.
7. Furber, S., ARM: system-on-chip architecture, 2nd Edition, Addison-Wesley, London, 2000.
8. Hayes, J. P., Computer Architecture and Organization, 3rd Edition, McGraw-Hill
9. Manuals- Intel 32/64 Architectures , ARM manual - 32/64-bit architecture, Intel 8051 and ATmega328P datasheet

References:

Online/E resources

1.

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT703	Course Name: CAD Algorithms for Synthesis of VLSI Systems
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment) 30%
(ii) Mid-term examinations 30%
(iii) End Semester Examination 40%

Course contents:

Unit 1: Introduction to CAD Algorithms

Role of CAD in digital system design, levels of design, modelling & description and support of languages, RTL, gate and system level synthesis; Technological alternatives and technology mapping

Unit 2: CAD Tools for synthesis

CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as micro-programmes, PLAs, gate arrays etc. Technology mapping for FPGAs. Low power issues in high level synthesis and logic synthesis.

Unit 3: Architectural-Level Synthesis and Optimization

Architectural Synthesis, Scheduling, Data path synthesis and control unit synthesis, scheduling algorithm, Resource Sharing and Binding

Unit 4: Logic-Level Synthesis and Optimization

Two-Level Combinational Logic Optimization, Multiple-Level Combinational Logic Optimization, Sequential Logic Optimization

Unit 5: CAD Algorithms for VLSI Physical Design

Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis.

Course Outcomes:

CO1. Is able to grasp various operations on graphs, clique, coloring, partitioning etc
CO2. & apply graph algorithms and its applications into Boolean function representation (Knowledge)
CO3. Is able to grasp graph models for architecture representation (Knowledge)
CO4. Is able to analyze & implement two level/Multilevel/ sequential logic synthesis algorithms
CO5. (approximate & exact algorithms) (skills)
CO6. Is able to analyze & implement library binding algorithms- FSM equivalence & optimization (skills)
CO7. To able to grasp core concept of VLSI Physical Design. (Knowledge)

Textbooks:

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.
4. N. Deo, Graph Theory, PH India.
5. Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
6. Sherwani, N. VLSI physical design automation. Kluwer, 1999.
7. Sarrafzadeh, M. and Wong, C. K. An introduction to VLSI physical design, Mc Graw Hill, 1996.

References:

8. Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z G. Field programmable Gate arrays. Kluwer, 1992.
9. Betz, V., Rose, J. and Marquardt, A. Architecture and CAD for Deep-submicron FPGAs. Kluwer, 1999.
10. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.

Online/E-resources:

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech. Embedded Systems	Department: Electronics & Communication Engineering
Course Code:ECT704	Course Name: Computer Vision
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

- Recognize and describe both the theoretical and practical aspects of computing with images.
- Grasp the principles, understanding of techniques, mathematical concepts and algorithms used in computer vision to facilitate further study in this area.
- Gain exposure to practical applications of computer vision in areas but not restricted to face recognition, object classification & detection, and video surveillance.
- Get an exposure to recent research areas in the field of computer vision and machine learning.

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit 1: Introduction and Overview: Overview of image processing systems, image formation and perception, continuous and digital image representation, image contrast enhancement, histogram equalization, affine transformations, model of image degradation/restoration process, Image Filtering

Unit 2: Feature Detection and Matching: Interest point detection, Edge, Blob, Corner detection; SIFT, SURF, HoG descriptors, Local Image Features and Feature Matching, RANSAC, Bag-of-words

Unit 3: Machine Learning and Deep Learning Quick course: Supervised & Unsupervised Machine Learning, Clustering , Classification, Review of Neural Networks, Convolutional Neural Network, CNN Architectures: AlexNet, VGG, InceptionNets, ResNets, DenseNets, Transfer Learning, Recurrent Neural Network, Long Short Term Memory(LSTM) , Visualization with CAM, Grad-CAM

Unit 4: CNNs for Computer Vision Tasks: Image Classification: CIFAR, MNIST, ImageNet Datasets, Object Detection: R-CNN, Fast R-CNN, Faster R-CNN, YOLO, SSD; Segmentation: FCN, U-Net, Mask-RCNN

Unit 5: Recent Trends and Applications: Deep Generative Models, Generative Adversarial Networks (GANs), Attention Models, Graph Convolutional Networks, Zero-shot, One-shot, Few-shot Learning, Visual Question Answering, Image Captioning

Course Outcomes:

At the end of the course students should be able to:

CO1: Describe different image representation, their mathematical representation and different their data structures used. (Cognitive-Remembering, Understanding)

CO2: Implement feature extraction techniques for developing computer vision applications (Skills - Apply, create)

CO3: Recognize the object using the concepts of machine vision (Cognitive + Skill- Analyze)

CO4: Grasp the principles of state-of-the-art deep neural networks (Skills- Apply, Evaluate)

CO5: Develop the practical skills necessary to build computer vision applications (Skills- Apply, Evaluate)

References:

1. Computer Vision: Algorithms and Applications, by Richard Szeliski
2. Computer Vision: A Modern Approach, Forsyth and Ponce, Pearson Education.
3. Christopher Bishop, Pattern Recognition and Machine Learning, Springer, 2008
4. Concise Computer Vision by Reinhard Klette
5. Deep Learning, by Goodfellow, Bengio, and Courville.
6. NPTEL Course DeepLearning for Computer Vision By Prof. Vineeth N Balasubramanian (IIT Hyderabad)

Online/E resources

Delivery plan

Unit	*Week (12 Weeks)*
Unit 1	Week 1, 2
Unit 2	Week 3, 4
Unit 3	Week 5, 6,7,8
Unit 4	Week 9,10
Unit 5	Week 11,12

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech (Embedded Systems)	Department: Electronics & Communication Engineering
Course Code: ECT910	Course Name: Modeling, Optimization & Transforms
Credit: 2	L-T-P: 2-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

[The following contents intend to cover implicit application to and exemplification through ECE problems in signal processing, probabilistic signal theory, optimization and soft-computing]

I. **Advancements in Transforms:** Discrete Fourier Transform, FFT, Short time Fourier Transform (STFT), Multi Resolution Analysis, Wavelet Transform, Continuous Wavelet Transform (CWT), Inverse CWT, Discrete Wavelet Transform, Sub-band coding and implementation of DWT, Applications (signal and image compression, de-noising, detection of discontinuous and breakdown points in signals), Discrete Cosine Transform, Stockwell-transform, Frequency selective filtering with wavelet and S-transform.

II. **Modelling:** Direct Modeling (identification), Inverse Modeling (Equalization), Classification and Clustering, Prediction/Forecasting, Auto regressive models (AR, MA, ARMA).

III. **Optimization:** Problem formulation, Linear Programming Problems, Solution by Graphical Methods, Symmetric Dual Problems, Slack and Surplus Variables, Simplex Method, Convex- Concave Problems.

IV. **Data Mining Techniques:** Higher Order Statistics, Principal Component Analysis, Linear Discriminant Analysis, Independent Component Analysis

Course Outcomes:

CO1. To learn the advancement in transforms
CO2. To understand the mathematical modeling and optimization techniques.
CO3. To learn the data mining techniques
CO4. To explore the engineering applications of the mathematical techniques.
CO5. To develop MATLAB and other programming skills for the mathematical techniques realization.

Textbooks:

1. Digital Signal Processing: Principles, Algorithms, and Applications 4 Edition, Author: John G. Proakis, Dimitris G Manolakis Publisher: Pearson.
2. Wavelets and Signal Processing, Author: Hans-Georg Stark, Publisher: Springer
3. The Wavelet Tutorial : The Engineer's Ultimate Guide to Wavelet Analysis, Author : Robi Polikar, University of Rowan : Online : http://users.rowan.edu/~polikar/WTtutorial.html
4. Stockwell, Robert Glenn, Lalu Mansinha, and R. P. Lowe. "Localization of the complex spectrum: the S transform." IEEE Transactions on Signal Processing 44.4 (1996): 998-1001.
5. Engineering Optimization: Theory and Practice, Third Edition SINGIRESU S. RAO, New Age Publishers
6. Data Mining - Concepts and Techniques, Authors : Jain Pei, Jiawei Han, Micheline Kamber, Publisher : Elsevier

References:

Online/E resources

1.

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT912	Course Name: Reduced order Modeling, Optimization & Machine intelligence
Credit: 2	L-T-P: 2-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment) 30%
(ii) Mid-term examinations 30%
(iii) End Semester Examination 40%

Course contents:

[The following contents intend to cover implicit application to and exemplification through ECE research problems in Electronic systems/Cognitive-systems domain such as reduced order polynomials, order reduction of a transfer function, sparse matrix based solution of large systems, discrete structures, implementation of search algorithms for design space exploration, and computer arithmetic implementation alongwith probabilistic reasoning for AI]

Unit-1: **Reduced order modelling & large Eigen value methods-** (i) (a) Large Matrix analysis and large Eigen value problem- Groups, fields and rings; vector spaces; basis & dimensions; canonical forms; inner product spaces- orthogonalization, Gram-Schmidt orthogonalization, unitary operators, change of orthonormal basis, diagonalization; (b) Eigenvalues & eigen vectors- Gerschghorin theorem, iterative method, Sturm sequence, QR method, introduction to large eigen value problems. 06 Hrs.

(ii) Reduced order modelling of systems- Taylor's polynomial, least square approximation, Chebyshev series/polynomial, curve fitting & splines, Pade & rational approximation 04 Hrs.

Unit-2: **Discrete Structures, algorithms & Combinatorial optimization**- counting methods, algorithm analysis, graph algorithms, dynamic algorithms, randomized algorithms, probabilistic algorithms, combinatorial optimization 10 Hrs.

Unit-3: **Digital arithmetic & machine intelligence-** (i) Number theory & computer arithmetic- unconventional number systems, residue number system, logarithmic number system, Chinese remainder theorem; fast evaluation of elementary & transcendental arithmetic functions. 06 Hrs.

(ii) Preface to AI- first order logic & inferencing, uncertainty, probabilistic reasoning systems, making decisions under uncertainty. 04 Hrs.

Course outcomes

CO1. Is able to grasp core concepts, basic tenets of linear algebraic structures- groups, fields and rings; vector spaces (knowledge)
CO2. Is able to grasp features, properties and operations on vector spaces- orthogonalization, change of basis, diagonalization (knowledge)
CO3. Is able to learn & apply problem solving for computing eigen values and eigen vectors etc. (Thinking, skills)
CO4. Is able to demonstrate application of algorithms (Gerschgorin, Sturm sequence method, QR method) for eigen value computation/estimation and MATLAB/SCILAB validation(skills)
CO5. Is able to describe algorithms for function approximation, fitting (rational, Chebychev, Pade etc.) using MATLAB (skills)
CO6. Develops appreciation for combinatorial optimization algorithms, AI probabilistic approaches & implements through MATLAB/C++/SCILAB (skills)

Textbooks: (not limited to)-

1. Schaum's outline on Linear Algebra, McGraw Hill
2. Topics in Algebra, I. N. Herstein, Wiley.
3. Advanced Model Order Reduction Techniques in VLSI Design, Sheldon Tan, Lei He, Cambridge Univ. Press, 2007.
4. Model Order Reduction: Theory, Research Aspects and Applications edited by W. H. A. Schilders, Henk A. Van Der Vorst, Joost Rommes, Springer.
5. Gerald, C F; Wheatley P O; Applied Numerical Analysis, Pearson, 2017
6. Theory and Applications of Numerical Analysis, G. M. Phillips, Peter J. Taylor, Academic press
7. Discrete Structures, Schaum outline
8. Cormen, Rivest, Leiserson, Introduction to Algorithms, PHI
9. Combinatorial optimization, Papadimitriou and Steiglitz, PHI (I)
10. Israel Koren, Computer Arithmetic- Academic Press

DPGC Convener Head, ECE SPGB Chairman

11. Russel and Norvig - Artificial Intelligence: A Modern Approach, Pearson, 3rd Ed. 2017

Further references:

1. Luigi FORTUNA, Guiseppe NUNNARI, Antonio GALLO, MODEL ORDER REDUCTION TECHNIQUES WITH APPLICATIONS IN ELECTRICAL ENGINEERING, Springer, 1992.
2. Y. Saad, Numerical methods for large Eigenvalue problems, www.umn.edu
3. Matrix Analysis & linear algebra, Meyer, SIAM
4. H. A. van der Vorst, Iterative methods for large linear systems, citeseerx.ist.psu.edu
5. Cheng et al, Symbolic analysis and reductions of VLSI circuits, Springer, 2005

Online/E resources:

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECP709	Course Name: Hardware Systems Lab
Credit: 2	L-T-P: 0-0-4
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	40%
(ii) Mid-term examinations	00%
(iii) End Semester Examination	60%

Course contents:

Problem-set for algorithm implementation:

Boolean algebraic formulations

a. Covering algorithm- Brach & bound
b. ROBDD computation
c. Operation between ROBDDs: '+', '.'

Graph based optimization

a. Two consideration each
b. Two consideration each
c. Graph coloring
d. Clique partitioning
e. Edge covering
f. Vertex covering
g. Independent set finding

List scheduling

a. Latency constrained resource minimization
b. Resource constrained latency minimization
c. Path based scheduling
d. Pipelined data-path scheduling
e. Hu's multiprocessor scheduling

Allocation & binding

a. FU binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
b. Storage unit binding
    a. Coloring
    b. Clique finding
    c. Left edge based binding
c. Interconnect binding
    a. Coloring
    b. Clique finding edge based binding

Course Outcomes:

CO1 Is able to describe ROBDD and implement minimization algorithm (Analyze, skill)
CO2 Is able to write & debug C-code for scheduling algorithms (skill)
CO3 Is able to write & debug basic algorithm for graph structures/features (skill)
CO4 Is able to write & debug C-code for binding/allocation algorithms (Skill)
CO5 Is able to implement digital circuits (datapath.control) on FPGAs for validation (create,skill)

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECP711	Course Name: Software Systems Lab
Credit: 2	L-T-P: 0-0-4
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	40%
(ii) Mid-term examinations	00%
(iii) End Semester Examination	60%

Course contents:

1. Design of software
   a) Assembly language programming
   b) Device drivers writing
   c) Object oriented interfacing,
   d) Debugging
2. Interfacing methods
3. Analog interfacing, data acquisition systems (board based)

Course Outcomes:

CO1 Is able to write & debug assemlby code (ARM) and mapon board (KEIL SW)
CO2 Is able to write device driver- keyboad, mouse, LCD, and program ports of ARM
CO3 Utilize CAD (Microvision/KEIL) for board mapping with sensors/transducer (skills)
CO4 Utilize GDB/Makefile for software writing

Texts:

References:

Online/E resources

DPGC Convener Head, ECE SPGB Chairman

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECP712	Course Name: System Design Lab
Credit: 2	L-T-P: 0-0-4
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment) 40%
(ii) Mid-term examinations 00%
(iii) End Semester Examination 40%

Course contents:

Group Application/Problems:

1. A-1 Layout Design- (i) Full adder, D-FF ; & (ii) synthesis of combinational & Sequential Components- 4-bit adder, 4-bit shift register, sequence detector ("1010")
2. A-2 Layout synthesis of already designed (1st Odd Semester) Data Path & Control for an arithmetic/logic application. Synthesis Using SYNOPSYS/CADENCE tool

Individual Application/Problems:

1. GCD-computer (4-bit)
2. Booth multiplier (4-bit)
3. 4-pt FFT
4. 4-pt IFFT
5. CORDIC for SinΘ/CosΘ
6. CORDIC for Sin-1Θ/Cos-1Θ
7. Non-Linear function exp(-2.5)/Sin 1.45/ Cos3.1/Sinh2.5/ Cosh3.2/log-natural
8. Find Average of Floating Point Numbers in Array of Size 16/32/64/128
9. For pseudo exhaustive TPG set T for BIST, follow the theorem concerning logical segmentation, which relates n (inputs), k (subspaces of size k among n), w (weight of n-tuple). Indicate w as well as |Tc| for different c; and n=20, k=3. Take example circuits/sub-systems for implementing the scheme & generating/applying random test patterns.
10. A circuit implementing f=xy+yz is to be tested using the syndrome-test method. Show that the faults z s-a-0 and z s-a-1 are not detected, while all other single stuck-at faults are detected. Arrange for experimental setup for all such testable as well as non-testable faults.
11. In a shift register polynomial division method of compression, a type 2 LFSR with P*(x)=1+x2+x4+x5 is to be used for input sequence 1 1 1 1 0 1 0 1 (8 bits). Compute signature for the input sequence. Indicate at least one more input sequence, which would alias the given sequence. Arrange for experimental setup for verifying your design.

Course Outcomes:

CO1. Is able to design layout of single stage amplifiers circuits using Cadence/open-source MAGIC tools (skills)
CO2. Is able to simulate and analyze data path/control using Cadence/Synopsys tools
CO3. Is able to generate/simulate test atterns using Cadence/Synopsys tools
CO4. Is able to write SystemC Modules (codes) for the various logic subsystems; Compile and Simulate using open-source SystemC compiler (knowledge, skills)

Text books:

References:

Online/E resources:

DPGC Convener Head, ECE SPGB Chairman

Program: M. Tech. (Embedded Systems)	Department: Electronics & Communication Engineering
Course Code: ECP 900	Course Name: Technical Documentation
Credit: 1	L-T-P: 0-0-2
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	40%
(ii) Mid-term examinations/Quizzes	20%
(iii) End Semester Examination	40%

Course contents::

Unit-1: Introduction: Literature survey – Understanding journal metrics (impact factor, number of citations, h-index, i10 index), Identifying high impact articles, Problem identification, Ethics of publishing.

(2 hours)

Unit-2: Document Formatting: Advantages of LaTeX, Installation, Package manager, Editors, Typesetting, Classes – Book, Thesis, Article, Slide, Poster, Parts of a document - Chapters, Sections, Items, Fonts, Acronyms, Author kits, Debugging.

(8 hours)

Figures, Tables, and Equations: Figures, Subfigures, Tables, Types of tables, Spacing in tables, Captions, Equations, Equation arrays, Equation numbering, Labels.

(8 hours)

Unit-3: Citing articles: Using labels, Citing articles, Bibliography management, Bibtex, Styles, Mendeley, JabRef.

(4 hours)

Unit-4: Artwork: Drawing with support in LaTeX- TikZ/pgf, Flowcharts in LaTeX, Creating plots with Gnuplot/ Octave/ Matlab, Creating scalable vector graphics with Inkscape, Tikz.

(4 hours)

Unit-5: Reviewing: Reformatting documents, Responding to reviewer comments, Reviewing technical documents.
(2 hours)

Course Outcomes – The students will be able to

1. Identify high impact literature, understand the importance of ethical publishing
2. Use LaTeX to compile technical documents containing quality figures, tables, and equations.
3. Use bibtex for automatic referencing.
4. Create quality graphics.
5. Understand the process of responding to reviewer comments, and reviewing technical documents.

Text books:

References:

1. **Khopka and Daly**, An introduction to Latex, Addison Wesley
2. **L. Lamport**, Latex

Online/E resources

https://www.anadolu.edu.tr/en/academics/faculties/course/99276/documentation-with-latex/content (3 credit) Anadolu University, Turkey
https://www.training.cam.ac.uk/course/ucs-latex (2 half days) Cambridge, UK
http://uva-fnwi.github.io/LaTeX/ (4 weeks) University of Amsterdam, Netherlands
https://www.bath.ac.uk/guides/getting-started-with-latex-an-introductory-course-for-doctoral-students/ (6 Hours) University of Bath, UK

DPGC Convener Head, ECE SPGB Chairman

Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT-616	Course Name: Computer Arithmetic & Micro-architecture Design
Credit: 3	L-T-P: 3-0-0

Pre-requisite course:

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course-contents:

Unit-1. Number theory & Computer arithmetic- conventional & unconventional number systems, residue & logarithmic number systems; Chinese remainder theorem; sequential & parallel (and high speed) algorithms for addition, multiplication, division; evaluation of elementary functions- sin, cos, $\sin^{-1}$, $\cos^{-1}$, sinh etc; CORDIC method for trigonometric functions.languages for design description (HDLs) like VHDL or Verilog;

Unit-2. Modeling and simulation of circuits at various levels;

Unit-3. Data path design for high performance- pipelining & systolic arrays; Control design- sequential, hardwired & micro-programmed control

Unit-4. Topics in design-yield and redundancy,

Unit-5. Low power design techniques.

Textbooks:

For Review

1. Kohavi, Switching & finite automata theory, Mc Graw Hill

Computer arithmetic

2. Ercegovac, Digital Systems, Wiely, 2004
3. Parhami, Computer Arithmetic- Algorithms & Hardware Design, Oxford Univ. Press
4. Koren, Computer Arithmetic Algebra, Prentice Hall Inc.

For Data-path/Control Design

5. Hayes, J P, Computer Architecture & organization, Mc Graw Hill, 2003

For HDLs

6. Navabi. Introduction to VHDL. Mc Graw Hill, 2000
7. Bhaskar. VHDL Primer. Prentice Hall India, 2001
8. Navabi. Verilog digital systems. Mc Graw Hill, 2000

Low power design

9. Mead & Conway, VLSI circuit design
10. Raguram, R. Modeling and Simulation of Electronic circuits. PHIndia, 1996.
11. Weste and Eshraghian. Principles of CMOS VLSI design. Addison Wesley, 1998.
12. K. Roy and et al, Low power design, Wiley

References:

1. Palnitkar, Verilog...., Pearson India/Prentice-Hall India
2. Chandrakasan, A. P. Low-power design methodologies. IEEE Press, 1998.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code:ECT618	Course Name: Graph Algorithms & Combinatorial Optimization
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1. Graph Theory- basics, Planarization, triangulation, graph algorithms for shortest/longest paths, spanning tree, search etc.

Unit-2. Optimization problem- Convex sets and functions.

Unit-3. The SIMPLEX algorithm- forms of linear programming problem, geometry of LP, organization of Tableau. Computational consideration for simplex algorithm

Unit-4. Duality- dual of LP, dual simplex problem. Primal-dual algorithm.

Unit-5. Algorithms & complexity- shortest path, max-flow, Dijkshtra's algorithm, min-cost flow, algorithm for graph search and matching; spanning trees and matroids; Integer Linear programming, Greedy algorithm, approximation algorithms; branch-and-bound; dynamic programming.

Course Outcomes:

CO1. Is able to grasp and analyze features, properties of graph entities e.g. cutset, tree, chord-set, cycles etc (Cognitive- Analyze)

CO2. Is able to learn & apply graph algorithms and its applications into Circuits, computer problem solving etc. (Skills- Analyze)

CO3. Is able in long perspective, to appreciate the significance of GRAPH as a versatile modeling entitiy; and the significance that it can be used for analysis, problem solving as well as synthesis- especially for chip design, wireless communication protocols & system design, computer problem solving, data structures etc. (Affective/Skills- Evaluate)

CO4. Is able to write small C/C++ programmes related to implementation of graph algorithms (Skills- Apply)

CO5. Is able to write efficient algorithms for graph-search, and other approximation algorithms (Skills, Evaluate)

Textbooks:

1. Narsingh Deo, Graph theory, Prentice Hall India, 2008.
2. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 2007
3. S. Baase, Computer algorithms, Pearson India 2008.
4. Papadimitriou and Steiglitz, Combinatorial optimization, PH India, 2001

References:

5. . Nemhauser and Wolsey, Integer and Combinatorial optimization, Wiley Inter-science 1999.

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT622	Course Name: System Level Design & Modeling
Credit:3	L-T-P:3-0-0

Pre-requisite Course: Embedded real-time system design and hardware/software interfacing (Embedded & Real-Time Systems, or equivalent)

Working knowledge of C/C++, algorithms and data structures (Data Structures, or equivalent)

Digital hardware design and hardware description languages (Digital System Design using VHDL, or equivalent).

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components:

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

UNIT 1. Introduction: Embedded systems, electronic system-level (ESL) design, Models of Computation (MoCs): finite state machines (FSMs), dataflow, process networks, discrete event

UNIT 2. System-level design languages (SLDLs): SpecC, SystemC. System specification, profiling, analysis and estimation. System-level design: partitioning, scheduling, communication synthesis

UNIT 3. System-level modeling: processor and RTOS modeling, transaction-level modeling (TLM) for communication. System-level synthesis: design space exploration (DSE)

UNIT 4. Embedded hardware and software implementation: synthesis and co-simulation, case study. Application specific processors, Retargetable compilers, instruction set-simulation and co-simulation.

UNIT 5. System design examples and case studies. . Recent trends in system level design and modeling

Course Outcomes:

A student is able to:

CO1- To model a problem at system level (Cognitive- Analyze)
CO2- Realize architecture for a design problem (Skills- Create)
CO3 -To model a system in System C language (Cognitive- Analyze)
CO4 -To generate system interface specifications and perform refinement (Skills- Create)
CO5- To appreciate HW-SW Co-design with latest trends (Cognitive- understanding)

Textbooks:

1. Gajski, S. Abdi, A. Gerstlauer, G. Schimer, Embedded System Design: Modeling, Synthesis, Verification, Springer, September 2009. ISBN 978-1-4419-0503-1, ("Orange book", authors' site).
2. Gerstlauer, R. Doemer, J. Peng, D. Gajski, "System Design: A Practical Guide with SpecC", Kluwer Academic Publishers, Boston, June 2001. ISBN 0-7923-7387-1 ("Yellow book")
3. T. Groetker, S. Liao, G. Martin, S. Swan, "System Design with SystemC", Kluwer Academic Publishers, Boston, May 2002. ISBN 1-4020-7072-1 ("Black book")
4. F. Vahid, T. Givargis, "Embedded System Design: A Unified Hardware/Software Introduction" (authors' site), John Wiley & Sons, 2001. ISBN 978-0-471-38678-0

References:

Online/E-resources:

R1. http://users.ece.utexas.edu/~gerstl/ee382v_f10/resources.html
R2. Latest journal papers for recent trends in system design

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT624	Course Name: VLSI Testing &Testability
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

UNIT 1.Introduction to VLSI design flow and need of VLSI testing. Physical Faults and their modeling; Stuck at Faults, Bridging Faults; Fault collapsing; Fault Simulation: Deductive, Parallel, and Concurrent Fault Simulation. Critical Path Tracing

UNIT 2.ATPG for Combinational Circuits: D-Algorithm, Boolean Differences, PODEM Random, Deterministic and Weighted Random Test Pattern Generation; Aliasing and its effect on Fault Coverage.

UNIT 3.PLA Testing, Cross Point Fault Model and Test Generation. Memory Testing- Permanent, Intermittent and Pattern Sensitive Faults, Marching Tests; Delay Faults.

UNIT 4.ATPG for Sequential Circuits: Time Frame Expansion ; Controllability and Observability Scan Design, BILBO , Boundary Scan for Board Level Testing ; BIST and Totally self checking circuits.

UNIT 5.System Level Diagnosis & repair - Introduction; Concept of Redundancy, Spatial Redundancy, Time Redundancy, Error Correction Codes. Latest trends in VLSI Testing and Testability

Course Outcomes:

At the end of the course the student will be able to:

CO1: To able to grasp core concepts of digital system testing and testability. (Cognitive - Understanding)

CO2: To understand how a faulty circuit may cause disasters and affect the nature as well as society. (Affective - Analyze Attitude & Value)

CO3: To understand fault detection using different fault simulation techniques. (Skills - Evaluate)

CO4: To develop ability to design algorithms for automatic test generation for combinational circuits, sequential circuits, PLAs and memory. (Skills/Affective - Create)

CO5: To apply probabilistic approaches for random test generation. (Skills - Apply)

CO6: To apply different redundancy based fault tolerance techniques to increase circuit reliability. (Skill/Affective - Analyze)

CO7: To design BIST for a CUT in Verilog/HDL and implement ATPG algorithms in C/C++/MATLAB. (Skills - Create)

Textbooks:

1. Abramovici, M., Breuer, M. A. and Friedman, A. D. Digital systems testing and testable design. IEEE press (Indian edition available through Jayco Publishing house), 2001.

References:

2. Bushnell and Agarwal, V. D. VLSI Testing. Kluwer.

3. Agarwal, V. D. and Seth, S. C. Test generation for VLSI chips. IEEE computer society press.

4. Hurst, S. L. VLSI testing: Digital and mixed analog/digital techniques. INSPEC/IEE, 1999.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT626	Course Name: Formal Verification of Digital Hardware & Embedded Software
Credit: 3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

UNIT 1. Introduction to Design Verification, OVM and UVM methodology, case studies using Verilog and System Verilog, Static verification,

UNIT 2. Formal Verification of digital hardware systems- BDD based approaches, functional equivalence, finite state automata, FSM verification, Model checking, Various industry & academia CAD tools for formal verification.

UNIT 3. Verification, validation & testing - Debugging techniques for embedded software, instruction set simulators, clear box technique, black box testing, evaluating function test

UNIT 4. Recent trends in Design verification, case study

Course Outcomes:

CO1: To understand features of System Verilog (Cognitive- Understanding)

CO2: To study Assertion Based Verification and also be aware of functional coverage. (Cognitive- Analyze/Evaluate)

CO3: To apply language constructs of Bluespec for high level design/synthesis. (Skills- Apply)

CO4: To understand the necessity of the verification methodology. (Affective- understanding)

CO5: Ability to develop the test bench for DUT with verification methodology for scheduling, resource sharing and binding.(Skills- Creativity)

Additonal/optional Outcomes:

6) Understand significance of formal verification methodologies vis-à-vis simulation/ABV (Knowledge)

7) To perform equivalence check for combinational as well as sequential digital circuits (Thinking)

8) To develop Kripe structure based Model for sequential circuits and write PROPERTIES for Model Checking (Thinking)

9) To be able to use Model checking CAD tool- SMV or Cadence/Synopsys tool (SMV or Formality) (Skills)

Textbooks:

1. Discrete Structures, Logic and Computability- James L. Hein, Jones & Barlett India.
2. Logic- Schaum Series
3. [Chapter 2, Micheli, Synthesis of Digital Systems, McGrawHill]
4. Articles by Bryant, Eap, Akers on BDDs.
5. Advanced Formal Verification, R. Drechsler, Kluwer.
6. Algorithms & Data structures in VLSI Design, C. Meinel and T. Theobald, Springer.

References:

1. SystemVerilog IEEE standard;
2. BlueSpec user guide/standard;
3. Embedded systems Design- Artist Roadmap for Research & Development, LNCS-3436, Springer.
4. J. W. Valvano, Embedded microcomputer systems- Real Time Interfacing, , Thomson press (Cengage India)
5. Computers as components- Principles of embedded computing system design. Wolf, W., Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II, New Delhi-110 048.)
6. Verification, validation & testing in software engineering, A. Dasso and A. Funes, Idea Group Inc.
7. Hardware-Software codesign for data flow dominated embedded systems, R. Niemann, Springer.
8. Readings in Hardware/Software codesign, Micheli, Ernst, Wolf, Morgan Kaufmann.
9. Advanced Formal Verification, R. Drechsler, Kluwer.
10. Readings in Hardware/Software codesign, Micheli, Ernst, Wolf, Morgan Kaufmann.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT628	Course Name: Memory Design & Testing
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Processing technology for Memories: Multipoly Floating Gate and Control Gate, Trench Capacitors and thin Oxide. Memory Modeling and testing faults in SRAMs, Marching Tests; Delay Faults.
Unit-2: Semiconductor memory architecture, Space of memory faults- fault primitives.
Unit-3: Preparation of Circuit Simulation: Definition & location of open, short, and bridge fault, Simulation methodology. Test for single cell and two port SRAMs, Functional fault modeling and testing of RAMS,
Unit-4: Fault Diagnosis & Repair Algorithms.
Unit-5: Built–in self-Test and design for testability of RAMs. Built in self repair architecture.
Unit-6: Trend in Embedded Memory testing.

Course Outcomes:

CO1: To know the basics of evaluation of elementary functions (Cognitive- Understand)

CO2: to understand fundamentals of Memory Modeling and testing faults (Cognitive- Understand)

CO3: To learn the techniques and algorithm for testing and fault diagnosis (Skills- Evaluate)

CO4: To understand basics of built-in self test and related issues (Skills- Design)

Textbooks:

References:

1. Pinaki Mazumder, Kanad Chakraborty, Testing and Testable Design of High-Density Random-Access Memories (Frontiers in Electronic Testing), Kluwer academic pub.
2. Said Hamdioui, Testing Static Random Access Memories: Defects, Fault Models and Test Patterns (Frontiers in Electronic Testing), Kluwer academic pub 2004.
3. Pinaki Mazumder and Kanad Chakraborty, Fault –Tolerence and reliability techniques for High –Density Random- Acess Memories, Pearson India, 2002.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code:ECT632	Course Name: Embedded SoC Design
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Interconnect (Bus, Arbiter etc.)
--Interconnects: AMBA, AHB, AXI; AXI Transaction Channels, Channel Timing, AXI interfaces, Network-on-Chip
Unit-2: IP Design, Development and Integration (Theory + Lab)
-- Custom IP Design, IP Packaging, IP Integration in a SoC
-- Verilog/VHDL for IP Design and Test
-- High Level Synthesis for IP Design and Test
Unit-3: Processor Architecture (any latest processor architecture, preferably Arm because of its dominance in SoC market) (Theory + Lab)
-- Arm Processor Architecture, Instruction Set Architecture, Memory Model, Case Study of Arm processor based SoCs
-- Programming of Arm Processors
Uni-4: System Level Integration of processor, interconnect and IP
-- Hardware-Software Integration
Uni-5: SoC Functional Testing/Verification
-- Unit/Module testing, Integration testing, Processor bring-up/boot-up, Test Pattern Generation
-- Timing Analysis, Functional Verification
-- Post Implementation (place & route) Timing and Functional Verification
Unit-6: Basic Device Driver Design
-- Concept of device driver for components; Revision of Embedded C programming
Unit-7: Introduction to Performance Analysis of SoC
-- Performance Analysis of SoC; Bandwidth of Buses; Data Transfer Rates
-- Average/Best Case/Worst Case Throughput Analysis
Unit-8: Advanced Modules (selective only):
1. System Level Modeling in SystemC
2. Scheduling on heterogeneous SoC
3. Hardware-Software Partitioning
4. Application Specific SoC Design using Case Studies like Bluetooth SoC
5. System Performance Analysis of SoC**Course Outcomes:**

Course outcomes: CO1: knowledge of embedded processors, RISC and CISC (Cognitive- Understand)
CO2: Basic concepts in CPU operation (Cognitive- Understand)
CO3: Understanding of I/O devices and their interfacing (Cognitive- Understand)
CO4: To learn program and system design and analysis methodologies (Skills- analyze and design)
CO5: Ability to reason about and understand a SoC
CO6: Ability to design a basic SoC using a tool like Vivado, Vivado HLS and Vivado SDK
CO7: Ability to create custom IP from a given specification

Textbooks:

1. System on Chip Design in Arm Cortex, Joseph Yiu
2. Arm System on Chip Architecture, Steve Furber
3. Zynq Book
4. Zynq Book Tutorials (with sources) for basic lab exercises
5. User guides from Xilinx for Vivado, Vivado HLS and Vivado SDK
6. User guides from Arm for Keil MDK and Arm DS-5
7. Wolf, W. Computers as components- Principles of embedded computing system design. Academic Press (Indian edition available from Harcourt India Pvt. Ltd., 27M Block market, Greater Kailash II, New Delhi-110 048.)

References:

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT634	Course Name: Micro- & Nano-Electro-Mechanical System (MEMS & NEMS)
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Introduction to MEMS: Introduction: micro- and nano-scale size domains; scaling of physical laws; MEMS materials and processes; Miniaturization Issues. MEMS devices and applications, MEMS Market **[4h].**

MEMS Fabrication Technology: Introduction to Submicron Technology: semiconductor materials; photolithography; doping; thin film growth and deposition; CVD, lithography and Ion Implantation, metallization; wet and dry etching; silicon micromachining; Bulk micromachining; Surface micromachining and LIGA **[4h].**

MEMS Sensors and Actuators (Electrostatic, Thermal, piezoresistive): mechanics including elasticity, beam bending theory, membranes/plates; microactuators based on various principles, electrostatic, thermal, piezoresistive and applications e.g. acceleration, strain, tactile, temperature, IR detector flow; inkjet **[10h].**

MEMS Sensors and Actuators (RF and Bio): MEMS Sensors and Actuators: mechanics including piezoelectric, magnetic, optical and its application. e.g. Microphone, micro speaker, nanogenerator, micro-motor, RF resonator, SAW filter. Materials and processes for BioMEMS, Applications **[10h].**

MEMS Devices Packaging and Calibration: MEMS device Calibration and packaging techniques, Reliability. MEMS software training: COMSOL & Intellisuite **[12h].**

Project

The class project is to design reasonably complex MEMS devices. The project will be performed as a team of two or three students

Course Outcomes:

At the end of the course the student will be able to:

CO1: Gain a knowledge of basic approaches for various MEMS sensors and actuators design. (Cognitive- understaning)

CO2: Capability to critically analyze microsystems technology for technical feasibility as well as practicality. (Affective- Evaluate)

CO3: Develop efficient design for improving device performance in terms of speed, sensitivity Selectivity and accuracy. (Skills- Create)

CO4: Design and optimization of RF MEMS sensors and actuators (Skills- Create)

CO5: Design and analysis of efficient MEMS presser sensor. (Skills- Analyze)

Textbooks:

1. Course notes – will be posted weekly on the course website

References:

2. Foundations of MEMS, Chang Liu, Prentice Hall (2006)
3. Fundamentals of Micro fabrication, Marc Madou, CRC (2002)
4. Introduction to BioMEMS – Albert Folch, CRC (2012)

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT634	Course Name: Micro- & Nano-Electro-Mechanical System (MEMS & NEMS)
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Introduction to MEMS: Introduction: micro- and nano-scale size domains; scaling of physical laws; MEMS materials and processes; Miniaturization Issues. MEMS devices and applications, MEMS Market **[4h].**

MEMS Fabrication Technology: Introduction to Submicron Technology: semiconductor materials; photolithography; doping; thin film growth and deposition; CVD, lithography and Ion Implantation, metallization; wet and dry etching; silicon micromachining; Bulk micromachining; Surface micromachining and LIGA **[4h].**

MEMS Sensors and Actuators (Electrostatic, Thermal, piezoresistive): mechanics including elasticity, beam bending theory, membranes/plates; microactuators based on various principles, electrostatic, thermal, piezoresistive and applications e.g. acceleration, strain, tactile, temperature, IR detector flow; inkjet **[10h].**

MEMS Sensors and Actuators (RF and Bio): MEMS Sensors and Actuators: mechanics including piezoelectric, magnetic, optical and its application. e.g. Microphone, micro speaker, nanogenerator, micro-motor, RF resonator, SAW filter. Materials and processes for BioMEMS, Applications **[10h].**

MEMS Devices Packaging and Calibration: MEMS device Calibration and packaging techniques, Reliability. MEMS software training: COMSOL & Intellisuite [12h].

Project

The class project is to design reasonably complex MEMS devices. The project will be performed as a team of two or three students

Course Outcomes:

At the end of the course the student will be able to:

CO1: Gain a knowledge of basic approaches for various MEMS sensors and actuators design. (Cognitive- understaning)

CO2: Capability to critically analyze microsystems technology for technical feasibility as well as practicality. (Affective- Evaluate)

CO3: Develop efficient design for improving device performance in terms of speed, sensitivity
Selectivity and accuracy. (Skills- Create)

CO4: Design and optimization of RF MEMS sensors and actuators (Skills- Create)

CO5: Design and analysis of efficient MEMS presser sensor. (Skills- Analyze)

Textbooks:

1. Course notes – will be posted weekly on the course website

References:

2. Foundations of MEMS, Chang Liu, Prentice Hall (2006)
3. Fundamentals of Micro fabrication, Marc Madou, CRC (2002)
4. Introduction to BioMEMS – Albert Folch, CRC (2012)

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT638	Course Name: Design of Asynchronous Sequential Circuit
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Introduction: Summary of synchronous techniques - disadvantages in today's technology. Advantages of asynchrononous techniques - low power, performance, modularity. Historic difficulties with asynchronous design. Flow Table Reduction, The state-assignment Problem, Delays, Hazards, and Analysis, Feedback, other Modes of operation, Counters.

Unit-2: Circuit Classification: Bounded Delay, speed independent, and delay independent. Data models (single-rail, dual-rail). Handshaking protocols (2 phase, 4 phase)

Unit-3: Micropipeline *Circuits*: Basic building blocks. Pipelines, with and without data processing elements. The design of the Amulet processors.

Unit-4: NCL Logic: The NULL convention logic approach. Preserving delay insensitivity, threshold gates with hysteresis.

Unit-5: Formal Aspects of Asynchronous: The Rainbow approach. Green descriptions of micro-pipelines. Overview of formal basis to asynchronous descriptions

Course Outcomes:

At the end of the course the student will be able to:

CO1- Gain a knowledge of asynchronous techniques. (Cognitive- understanding)

CO2-Evalvate delays and hazards in asynchronous design. (Affective- Evaluate)

CO3 –Analyze different method for improving digital design. (Skills- analyze)

CO4- Design and optimization of NCL logic. (Skills- Create)

Textbooks:

References:

1. Asynchronous sequential circuits by Stephen H. Unger, John Wiley & Sons
2. Switching and Finite Automota Theory. Kohavi, Tata McGraw Hill

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT642	Course Name: FPGA's Physical Design
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Introduction to FPGA Architectures.

Unit-2: FPGA design flow, partitioning,

Unit-3: Placement and

Unit-4: Routing algorithms.

Unit-5 Technology mapping for FPGAs, case studies.

Course Outcomes:

At the end of the course the student will be able to:

CO1- Gain a knowledge of different FPGA Architectures (Cognitive- understanding)

CO2- Understand challenges in placement and routing algorithms. (Cognitive - understanding)

CO3 –Analyze different method for improving physical design. (Skills- analyze)

CO4- Evaluate Technology mapping for FPGAs (Skills- Evaluate)

Textbooks:

References:

1. Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z G. Field programmable Gate arrays. Kluwer, 1992.
2. Betz, V., Rose, J. and Marquardt, A. Architecture and CAD for Deep-submicron FPGAs. Kluwer, 1999.
3. Trimberger, S. M. FPGA Technology. Kluwer, 1992.
4. Oldfield, J. V. and Dorf, R. C. FPGAs: Reconfigurable logic for rapid prototyping and implementation of digital systems. John Wiley, 1995

Online/E-resources:

Program: M. Tech. Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT648	Course Name: Languages for Hardware Description, Scripting and Simulation
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents: Combined syllabus of ECT648A, 648B and 648C

UNIT-I UNIX and SCRIPTING

Introduction to UNIX commands, Handling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection, Working on Vi/Vim/gvim editor, Basic Shell Programming, TCL, Perl and Python Scripting language.

UNIT-II HDL Simulation and Synthesis

Synthesis and simulation using HDLs- Logic synthesis using Verilog. FSM synthesis, Continuation, Data path Synthesis, Performance driven synthesis, Types of simulation, Problem solving, Static timing analysis. Formal verification, Switch level and transistor level simulation, Problem solving, Tutorial.

UNIT-III VLSI Design Verification (Selected Topics)

System Verilog- Introduction- Design hierarchy, Data types, Operators and language constructs, Functional coverage, Assertions, Interfaces and test bench structures, Assertions, Interfaces and test bench structures, OVM, UVM. Discussions.

UNIT-IV Verilog –A and Verilog- AMS

Analog/Mixed Signal Modeling and Verification-Introduction, Analog/Mixed signal modelling using Verilog-A, Analog/Mixed signal modelling using Verilog-AMS, Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling, Analog/Digital Boundary Issues: boundary issues coverage

UNIT V Advances in Scripting and System design

New softwares/languages recently used in industry. Case studies.

Course Outcomes:

At the end of the course the student will be able to:

CO1: execute the special features of VLSI back end and front end CAD tools and UNIX shell script

CO2: design synthesizable Verilog and VHDL code.

CO3: Application of Verilog and system Verilog in digital system

CO4: Model Analog and Mixed signal blocks using Verilog A and Verilog AMS

CO5: Understand the new scripting languages,system design softwares and EDA tools.

Textbooks:

References:

1. S. Sutherland, S. Davidmann, P. Flake, "System Verilog for Design (2/e)" Springer,2006.
2. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2008.
3. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
4. Recent literature in Electronic Design Automation Tools.
5. Z. Dr Mark, "Digital System Design with SystemVerilog", Pearson 2010;

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT652	Course Name: RF MEMS
Credit:	L-T-P:
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

RF MEMS relays and switches: Switch parameters, Actuation mechanisms, Bistable relays and micro actuators, Dynamics of switching operation.

MEMS inductors and capacitors: Micromachined inductor, Effect of inductor layout, Modeling and design issues of planar inductor, Gap tuning and area tuning capacitors, Dielectric tunable capacitors.

Micromachined RF filters: Modeling of mechanical filters, Electrostatic comb drive, Micromechanical filters using comb drives, Electrostatic coupled beam structures.

MEMS phase shifters: Types, Limitations, Switched delay lines, Micromachined transmission lines, Coplanar lines, Micromachined directional coupler and mixer.

Micromachined antennas: Microstrip antennas – design parameters, Micromachining to improve performance, Reconfigurable antennas.

Course Outcomes:

At the end of the course the student will be able to:

CO1: Understand various parameters of RF MEMS Switch and its actuation
CO2: Model and design inductor and capacitors
CO3: Design Micromechanical filters
CO4: Understand the various aspects of design of MEMS phase shifters and its application
CO5: Analyze the performance of microstrip antennas

Textbooks:

References:

1. H.J.D.Santos, "RF MEMS Circuit Design for Wireless Communications", Artech House ,2002.
2. G.M.Rebeiz , "RF MEMS Theory , Design and Technology", wiley , 2003.
3. Stephen D Senturia, "Microsystem Design", Kluwer Academic Publishers, 2001.
4. Marc Madou, "Fundamentals of Microfabrication", CRC Press, 1997.
5. V.K.Varadan, K.J Vinoy & K.A. Jose, "RF MEMS and their Applications", Wiley,2003.
6. Gregory Kovacs, "Micromechanised Transducers Source Book", WCB McGraw Hill, Boston, 1998.
7. M H Bao, "Micromechanical Transducers, Pressure Sensors, Accelerometers and Gyroscopes" Elsevier, Newyork, 2000.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code:ECT654	Course Name: RF Integrated Circuit
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Fundamental concepts in RF Design – harmonics, gain compression, desensitization, blocking, cross modulation, intermodulation, inter symbol interference, noise figure, Friis formula, sensitivity and dynamic range;

Unit-2: Receiver architectures – heterodyne receivers, homodyne receivers, image-reject receivers, digital-IF receivers and subsampling receivers; Transmitter architectures – direct-conversion transmitters, two-step transmitters;

Unit-3: Low noise amplifier (LNA) – general considerations, input matching, CMOS LNAs; Down conversion mixers – general considerations, spur-chart, CMOS mixers; Oscillators – Basic topologies, VCO, phase noise, CMOS LC oscillators;

Unit-4: PLLs – Basic concepts, phase noise in PLLs, different architectures.

Course Outcomes:

CO1: Knowledge of basic concepts in RF integrated circuit design (Cognitive- understanding)
CO2: Acquaintance with various architectures of receivers and transmitters (Cognitive- Analyze)
CO3: Awareness of several concepts of low noise amplifiers (Cognitive- understanding)
CO4: Knowledge of applications of mixers, oscillators and PLLs. (Skills- Applying)

Textbooks:

1. Behzad Razavi, RF Microelectronics, Prentice Hall PTR, 1997

References:

2. Thomas H. Lee, The design of CMOS radio-frequency integrated circuit, Cambridge University Press, 2006

3. Chris Bowick, RF Circuit Design, Newnes, 2007.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT656	Course Name: Adaptive Signal Processing
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Introduction to Adaptive systems, Adaptive Linear combiner, Minimum Mean-Square Error, Wiener-Hopf Equation, Error Performance Surface, LMS algorithm, Convergence of weight vector, Learning Curve, FX-LMS algorithm (Filtered X-LMS) and its application to ANC, Types of LMS, RLS algorithm, Matrix Inverse Lemma for RLS, Computational complexity of LMS and RLS, Convergence Analysis.

Unit-2: IIR-LMS, Lattice Filter, FIR to Lattice conversion and vice-versa, Adaptive Lattice Filter

Unit-3: Kalman Filter, Adaptive Kalman Filter

Unit-4: Transformed domain adaptive filtering : Block Linear, Block Circular

Unit-5: Filter Banks and multi-rate signal processing

Unit-6: Distributed signal Processing : Incremental LMS, Diffusion LMS

Course Outcomes:

CO1 : To learn the characteristics of adaptive system architecture and analyze Wiener-Hopf Equation.

CO2 : To understand the machine learning algorithms including LMS, RLS, Fx-LMS etc.

CO3 : To learn the adaptive structures like : Adaptive Lattice Filter, Kalman Filter, Transformed domain adaptive filtering, Filter Banks.

CO4 : To explore the applications of adaptive signal techniques to System Identification, Channel Equalization, time series prediction etc.

CO5 : To develop MATLAB programming skills for adaptive systems.

Textbooks:

References:

1. B. Widrow and S. D. Stearns : Adaptive Signal Processing, Prentice Hall.
2. D. G. Manolakis, V. K. Ingle, S. M. Kogon : Statistical and Adaptive Signal Processing, McGraw Hill.
3. S. S. Haykin : Adaptive Filter Theory, 4th Edition, Prentice Hall.
4. A. H. Sayed : Fundamentals of Adaptive Filtering, John Wiley & Sons.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code:ECT657	Course Name: VLSI Signal Processing Architectures
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit 1: Introduction to VLSI DSP Systems

Need of VLSI DSP algorithms. Main DSP Blocks and typical DSP Algorithms. Fixed point /Floating point Representation; Floating point Arithmetic Implementation, Architectures of Adders/Multipliers; CORDIC, representation of DSP algorithms: Block Diagram, signal flow graph, data flow graph, dependence graph.

Unit 2: Iteration Bound

Data flow graph representations, loop bound and iteration bound, longest path matrix algorithm, iteration bound of Multi-rate data flow graphs

Unit 3: Pipelining and Parallel Processing:

Pipelining and parallel processing of FIR digital filters, pipeline interleaving in digital filters: signal and multichannel interleaving

Unit 4: Retiming, Unfolding and Folding:

retiming techniques; algorithm for unfolding, Folding transformation, Techniques of retiming, Unfolding & Folding

Unit 5: Systolic Array Architecture

Systolic Array Architecture: Methodology of systolic array architecture, FIR based Systolic Array, Selection of Scheduling Vector, Matrix multiplication of systolic array

Unit 6: Low power Design

Theoretical background , Scaling v/s power consumption, power analysis, Power reduction techniques, Power estimation approach

Course Outcomes:

CO1: To understand Graphical representation of DSP algorithms and Mapping algorithms into Architectures (Cognitive/Skills - Apply)

CO2: To study architecture for real time systems and parallel and pipelining for Low power design (Cognitive- Remembering)

CO3: To be aware of systolic Array architecture and methodology for developing Architectures (Cognitive - Understanding)

CO4: To know different signal processing modules as convolution technique, retiming concept, folding /unfolding Transformation and CORDIC architecture. (Cognitive- Analyze)

CO5: To implement different low power Design techniques. (Skills - evaluate)

Textbooks:

1. VLSI Digital Signal Processing System : : Design and implementation by K.K. Parhi

References:

2. Digital Signal Processing with Field Programmable Gate Arrays Uwe Meyer-Baese , Springer.
3. FPGA-based Implementation of Signal Processing Systems. by Roger Woods, John Mcallister, WILEY

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code:ECT662	Course Name: Advanced Digital Signal & Image Processing
Credit:	L-T-P:
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Introduction to Multirate systems and filter banks, 2D systems and mathematical Preliminaries, Digital Representation of Binary & Gray Scale and color Images, Linear operations on images.
Image sampling and quantization: 2D Sampling on rectangular and nonrectangular sampling lattice, Aliasing, Lloyd-Max quantizer etc.
Image Transforms: 2D Discrete Fourier transform, DCT, DST and Hadamard, Harr K-L Transforms & their applications to image processing.
Image restoration: Wiener filtering , smoothing splines and interpolation.
Image Enhancement Techniques: Gray scale transformation, Histogram matching and equalization, Smoothening:- Noise Removal, Averaging, Median, Min/Max. Filtering sharpening of Images using differentiation, the Laplacian, High Emphasis filtering.
Image analysis: Edge detection, Boundary Lines & Contours.
Image representation by Stochastic models: ARMA models, 2D linear prediction.
Image Segmentation &Thresholding: Multiband Thresholding, Thresholding from Textures, Selective histogram Technique.
Image Compression: Compression Techniques using K-L Transform, Block Truncation Compression. Error free Compression using Huffman coding & Huffman shift coding.

Course Outcomes:

CO1 : Ability to understand Multirate systems , Image sampling and quantization
CO2 : Ability to understand Image Transforms , Image restoration and Image Enhancement Techniques
CO3 : Ability to understand Image analysis , Image Segmentation &Thresholding, Image Compression

Textbooks:

1. Digital Signal Processing- Oppenheim A.V. & Schafer R.W. PHI.
2. Digital Signal Processing-by Mitra- (TATA McGraw Hill) Publications.
3. Digital Image Processing- by Gonzalez / Woods, (Pearson Education)
4. Digital Image Processing- by A.K. Jain

References:

5. Digital Picture Processing- by Rosenfield & Kak

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT690	Course Name: Wireless Sensor Networks
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Network architecture, wireless communication: the physical layer in WSN,

Unit-2: WSN medium access control and link layer protocols,

Unit-3:WSN services: synchronization and localization, topology control and routing, data-centric and content-based routing,

Unit-4: Quality of Service and transport protocols, in-network aggregation and WSN security

Course Outcomes:

CO1 : Master the fundamentals of wireless sensor network.

CO2: Understand the protocols and their design considerations.

CO3 : Model and simulate different WSN parameters.

CO4 : Understand the parameters to estimate the QoS.

CO5: Master key routing protocols and the associated design challenges.

Textbooks:

1.Murthy & Manoj, "Ad Hoc Wireless Networks: Architectures and Protocols," ISBN 0-13- 147023-X, Pearson 2004

2. William Stallings, "Wireless Communications & Networks", ISBN: 0131918354, Prentice Hall; 2nd edition, November 12, 2004.

References:

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT703	Course Name: CAD Algorithms for Synthesis of VLSI Systems
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit 1: Introduction to CAD Algorithms

Role of CAD in digital system design, levels of design, modelling & description and support of languages, RTL, gate and syste m level synthesis; Technological alternatives and technology mapping

Unit 2: CAD Tools for synthesis

CAD tools for synthesis, optimization, simulation and verification of design at various levels as well as for special realizations and structures such as micro-programmes, PLAs, gate arrays etc. Technology mapping for FPGAs. Low power issues in high level synthesis and logic synthesis.

Unit 3: Architectural-Level Synthesis and Optimization

Architectural Synthesis, Scheduling, Data path synthesis and control unit synthesis, scheduling algorithm, Resource Sharing and Binding

Unit 4: Logic-Level Synthesis and Optimization

Two-Level Combinational Logic Optimization, Multiple-Level Combinational Logic Optimization, Sequential Logic Optimization

Unit 5: CAD Algorithms for VLSI Physical Design

Introduction to VLSI Physical Design flow. Circuit partitioning, placement and routing algorithms. Design Rule-verification, Circuit Compaction; Circuit Extraction and post layout simulation. FPGA design flow- partitioning, placement and routing algorithms. Deep sub-micron issues; interconnects modeling and synthesis.

Course Outcomes:

CO1. Is able to grasp various operations on graphs, clique, coloring, partitioning etc
CO2. & apply graph algorithms and its applications into Boolean function representation (Knowledge)
CO3. Is able to grasp graph models for architecture representation (Knowledge)
CO4. Is able to analyze & implement two level/Multilevel/ sequential logic synthesis algorithms
CO5. (approximate & exact algorithms) (skills)
CO6. Is able to analyze & implement library binding algorithms- FSM equivalence & optimization (skills)
CO7. To able to grasp core concept of VLSI Physical Design. (Knowledge)

Textbooks:

1. G. D. Micheli. Synthesis and optimization of digital systems.
2. Dutt, N. D. and Gajski, D. D. High level synthesis, Kluwer, 2000.
3. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.
4. N. Deo, Graph Theory, PH India.
5. Sait, S. M. and Youssef, H. VLSI Physical design automation. IEEE press, 1995.
6. Sherwani, N. VLSI physical design automation. Kluwer, 1999.
7. Sarrafzadeh, M. and Wong, C. K. An introduction to VLSI physical design, Mc Graw Hill, 1996.

References:

8. Brown, S. D., Francis, R. J., Rose, J. and Vranesic, Z G. Field programmable Gate arrays. Kluwer, 1992.
9. Betz, V., Rose, J. and Marquardt, A. Architecture and CAD for Deep-submicron FPGAs. Kluwer, 1999.
10. T. H. Cormen, C. E. Leiserson and R. L. Rivest, "Introduction to Algorithms," McGraw-Hill, 1990.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECP706	Course Name: Advanced Embedded Software Design
Credit:3	L-T-P:3-0-0

Pre-requisite Course:

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Processor micro-architecture, application-specific architecture,

Unit-2: Embedded OS, middleware, graphics libraries,

Unit-3: Software Development Tools, graphics IPs, virtual prototyping solutions,

RTOS, Embedded linux, concurrency & concurrent programming languages;

Unit-4: Design automation of such systems including methodologies, techniques and tools for their design as well as novel designs of software components

Course Outcomes:

CO1. Is able to grasp core concepts, basic tenets of micro-architecture vis a vis embedded operating systems, Unix shell programming (Cognitive- understanding) PO1

CO2. Is able to grasp features, properties of Embedded OS(Cognitive- understanding) PO1

CO3. Is able to learn & apply scheduling, deadlock avoidance algorithms and its applications into process scheduling, deadlock avoidance related problem solving etc. (Skills- evaluate) PO2, PO4, PO5, PO11

CO4. Is able in long perspective, to appreciate the significance of virtual memory, file management, security & privacy in OS (Skills- Analyze) PO1, PO4, PO12

CO5. Is able to write programmes for RTOS- scheduling, concurrency, deadlock prevention, etc.; and the significance that it can be used for analysis, problem solving as well as design of OS kernels (Skills- Evaluate) PO5

CO6. Is able to use Embedded OS CAD tools & development environment- VxWorks Windriver, RTLinux, Micrivision (ARM) (Skills- Create) PO2, PO13

Textbooks:

1. Unix Shell Programming, Kernighan & Pike, PHI
2. Lex & Yacc
3. Linux for Embedded and Real-time Applications, Doug Abbott, Newnes, Elsevier, 2003.
4. An Embedded Software Primer, David E. Simon, Addison Wesley, 1999.
5. Embedded Linux, Pearson.
6. Operating systems principles, Silberchatz, Galvin, Wiley
7. Short, K, Embedded Microprocessor System Design, Prentice Hall, 1998.
8. Embedded Linux, Pearson
9. Edward A. Lee, "Embedded Software", Advances in Computers (M. Zelkowitz, editor) 56, Academic Press, London, 2002.
10. Testing Embedded Software, by Bart Broekman and Edwin Notenboom, Pearson/Addison-Wesley (UK), ISBN: 0-321-15986-1

References:

11. Design Patterns for Embedded Systems in C: An Embedded Software Engineering, Bruce Powel Douglass, Newnes, Elsevier.
12. Software Engineering for Embedded Systems: Methods, Practical Techniques, Robert Oshana, Mark Kraeling, Newnes, Elsevier.
13. Embedded Software, Newnes know it all series, Jean J. Labrosse, ISSN 1879-8683, Elsevier.
14. Programming Embedded Systems in C and C++, O'Reilly Series, Michael Barr.
15. Real-Time Concepts for Embedded Systems, CMP books, R and D Developer Series, Qing Li, Caroline Yao, CRC press.
16. Testing Embedded Software, Broekman Bart, Pearson Education India, ISBN 813172509X, 9788131725092.
17. Performance Analysis of Real-Time Embedded Software, Yau-Tsun Steven Li, Sharad Malik, Kluwer.
18. Embedded Software for SoC, Ahmed Amine Jerraya, Springer.

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT733	Course Name: Pattern Analysis & Machine Intelligence
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

UNIT I

Introduction to Pattern Recognition and Machine Learning, ML design cycle, types of learning: supervised, unsupervised and reinforced, introduction to feature extraction and classification, density and discriminant functions, decision surfaces.

Review of probability theory: conditional probability, Bayes theorem, random variables, density and mass functions, expectation and variance, joint distribution function of multiple random variables, multivariate normal distribution.

UNIT II

Bayesian decision theory, Bayes Classifier, Naïve Bayes classifier, Euclidian distance and Mahalanobis distance-based classifiers, minimum-error-rate classification. Parameter estimation methods, Maximum-Likelihood estimation, Gaussian mixture models, Expectation maximization method, Bayesian estimation,

Hidden Markov models for sequential pattern classification: discrete hidden Markov models, continuous density hidden Markov models.

UNIT III

K-nearest neighbour classification: Simple and distance weighed voting approach. Support vector machines: linear SVM, soft-margin approach for non-separable data, kernel trick to learn non-linear SVM, radial basis function, polynomial, and sigmoidal kernel. Decision tree classifier: set of questions, splitting criterion, stop-splitting rule, and class assignment rule in decision tree. Introduction to neural networks: perceptron as linear classifier and multi-layer perceptron. Regression Analysis.

UNIT IV

Feature extraction methods: statistical features, Fourier and wavelet transforms for feature extraction, Data transformation and dimension reduction: Fisher's linear discriminant analysis, Bayesian LDA, step-wise LDA, principal component analysis, kernel-PCA. Optimization in feature selection. Feature visualization.

Ensemble of classifiers. Evaluation the performance of a classifier: holdout, random sampling, and cross validation methods, sensitivity, specificity, confusion matrix and ROC curve. Multi-class classification. Statistical analysis for comparison of significance of multiple classifiers over multiple dataset: Template matching and context dependent classification. The curse of dimensionality.

UNIT V

Unsupervised learning and clustering. Criterion functions for clustering. Prototype-based, Graph-based, Density-based clusters. Algorithms for clustering: K means, DBSCAN, Hierarchical clustering, Cluster validation.

Course Outcomes:

The course equips the students with strong basics in Pattern Recognition and Machine Learning (ML).

CO1: The students would have exposure to different algorithms for learning pattern classification methods and would also have explore to different datasets to get a feel for ML algorithms.

CO2: The statistical and mathematical formulation underlying different algorithms would be understood.

CO3: A background needed to study more advanced topics in ML will be developed (e.g. Deep Learning, Generative Adversarial Networks, etc.).

CO4: The course would help students to build a career in industry using ML, or to be a data scientist, or to pursue research in ML.

Textbooks:

Reference Text-Books

1. R. O. Duda, P. E. Hart and D. G. Stork, **Pattern Classification**, John Wiley, 2001
2. S. Theodoridis and K. Koutroumbas, **Pattern Recognition**, 4th Ed., Academic Press, 2009
3. C. M. Bishop, **Pattern Recognition and Machine Learning**, Springer, 2006
4. T. Pang-Ningm, V. Kumar, M. Steinbach. **Introduction to data mining.** Pearson Education India, 2018.

Programming Books

5. S. Theodoridis *et. al.*, **'Introduction to Pattern Recognition, A MATLAB Approach'**. Academic Press, 2010

References:

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT 734	Course Name: Internet of Things & IIoT
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

i) **Introduction to IoT**;
IoT sensors, devices, networks & protocols; Cyber physical Systems

ii) **IoT programming & big data**
Machine-to-Machine Communications; Interoperability in IoT, Introduction to Arduino Programming; Integration of Sensors and Actuators with Arduino; Introduction to Python programming, Introduction to Raspberry Pi, Implementation of IoT with Raspberry Pi; Data Handling and Analytics, Cloud Computing;

iii) **Cybersecurity & privacy in IoT** (optional)

iv) **Low energy, secure hardware for IoT/sensors**

v) **Global applications** (selected only)
Smart Cities and Smart Homes; Connected Vehicles, Smart transportation; Smart Grid, Industrial IoT; Case Study: Agriculture, healthcare including Smart monitoring of critical diseases & point of care; Activity Monitoring, supply chain & semiconductor manufacturing;

vi) **Industrial IoT (IIoT)**: (selected only)
Enabling Factors: CPS, Energy Market; Example Deployment: Building Automation; Automotive and Transportation; Industrial (Manufacturing); building automation, agriculture, Oil & Gas; RTOS; Network Functions Virtualization; Long-range Wireless Protocols; LoRa WAN; Satellite Communications; ANT+, WiFi, ZigBee, WHART, EnOcean, Z-Wave, NFC; SECURITY: Encryption algorithms- Diffie-Hellman, Encryption Algorithms; Threat Vectors, Attacks: Man-in-the-middle, Replay, Protection Methods, Side-Channel Attacks, Chain of Trust; Hash and MAC Functions; Secure Firmware Updates, Random Number Generation; Predictive and Preventive Maintenance, IIOT deployment and Industrial Internet

Course Outcomes:

CO1. Able to grasp the concept of IoT and embedded systems, cyber physical systems

CO2. Exposing for the end-to-end design of Internet-of-Things applications from sensors to cloud, as well as hardware design/security aspects

CO3. Building in confidence and capability regarding electronics, sensors, and software through hands-on labs.

CO4. Providing exposure to practical problems and their solutions, through case studies using EDA Tools (Electronic Design Automation tools).

Enhancing the knowledge to Security and privacy needs, and the analysis required to address these needs.

References:

1. "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", by Pethuru Raj and Anupama C. Raman (CRC Press)
2. "Internet of Things: A Hands-on Approach", by Arshdeep Bahga and Vijay Madisetti (Universities Press)

Online/E-resources:

Program: M Tech in Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT735	Course Name: Probabilistic Machine Learning and Artificial Intelligence
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Unit-1: Knowledge & Reasoning- Agents, First order logic & inference; Knowledge representation;
Uncertain Knowledge & reasoning- Uncertainty, probabilistic reasoning & reasoning over time; simple & complex decisions;
Learning- Learning from observations, Statistical learning methods, Reinforcement learning;
Applications- Probabilistic language processing, perception, Robotics
AI Fundamentals- Fundamental Concepts of AI: Agents, environments, general model; Problem Solving techniques.
Search Techniques- Uninformed search, heuristic search, adversarial search and game trees; Solution of constraint satisfaction problems using Search.

Unit-2: Knowledge Representation- Propositional and predicate calculus, semantics for predicate calculus, inference rules. reasoning with propositional and predicate logic,

Unit-3: Machine Learning Structures- Supervised and unsupervised learning. Artificial Neural Network (Multi-Layer Perception), Radial Basis Function, Functional Link ANN, Self-Organizing Map, Clustering Adaptive FIR and IIR structures.
Machine Learning - Least Mean Square algorithm, Back Propagation, Genetic algorithm, Algorithms Differential Evolution, Particle Swarm Optimization and Other Nature Inspired Optimization.
Decision under uncertainty; probabilistic inferencing;

Unit-4: Algorithmic models of learning. Learning classifiers, functions, relations, grammars, probabilistic models, value functions, behaviors and programs from experience. Bayesian, maximum a posteriori, and minimum description length frameworks. Parameter estimation, sufficient statistics, decision trees, neural networks, support vector machines, Bayesian networks, bag of words classifiers, N-gram models; Markov and Hidden Markov models, probabilistic relational models, association rules, nearest neighbor classifiers, locally weighted regression, ensemble classifiers.

Unit-5: Computational learning theory, mistake bound analysis, sample complexity analysis, VC dimension, Occam learning, accuracy and confidence boosting. Dimensionality reduction, feature selection and visualization. Clustering, mixture models, k-means clustering, hierarchical clustering, distributional clustering. Reinforcement learning; Learning from heterogeneous, distributed, data and knowledge. Selected applications in data mining, automated knowledge acquisition, pattern recognition, program synthesis, text and language processing, internet-based information systems, human-computer interaction, semantic web, and bioinformatics and computational biology.

Course Outcomes:

CO1. Upon completion of this programme, participants will be able to:
CO2. Decide whether AI & ML techniques are applicable for a given business problem and articulate its benefits thereof
CO3. Formulate business problems as AI & ML problem
CO4. Collect data and apply pre-processing techniques
CO5. Apply Supervised Learning, Unsupervised learning, Deep Learning, Visualization techniques
CO6. Identify appropriate techniques to solve the formulated AI & ML problem
CO7. Implement and compare the relevant algorithms using Python
Interpret and present the predicted model

Textbooks:

1. Pattern Recognition and Machine Learning by Chris Bishop
2. Bayesian Data Analysis by Gelman, Carlin, Stern, & Rubin
3. Machine Learning: A Probabilistic Perspective by Kevin Murphy [be sure to get the fourth printing; there were many typos in earlier versions]
4. Bayesian cognitive modeling: A practical course by Michael Lee and Erik-Jan Wagenmakers [electronic version online]
5. Russel Norvig- Artificial intelligence : A modern Approach, Pearson.

References:

6. Modeling and Reasoning with Bayesian networks by Adnan Darwiche.
7. Pattern Recognition and Machine Learning by Chris Bishop.
8. Machine Learning: a Probabilistic Perspective by Kevin P. Murphy.
9. Information Theory, Inference, and Learning Algorithms by David J. C. Mackay. Available online.
10. Bayesian Reasoning and Machine Learning by David Barber. Available online.

11. Graphical models, exponential families, and variational inference by Martin J. Wainwright and Michael I. Jordan. Available online
12. [CI] Programming Collective Intelligence by Toby Segaran, O'Reilly Media, 2007, ISBN: 0596529325 ^
13. [ML] Marsland. (2009). Machine Learning: An Algorithmic Perspective. By Marsland, CRC Press, 2009. ^

Online/E-resources:

14. [PY] How to Think Like a Computer Scientist: Learning with Python 2ed by Jerey Elkner, Allen B. Downey and Chris Meyers (Open Book Project) http://www.greenteapress.com/thinkpython/

Program: M Tech (Embedded Systems)	Department: Electronics & Communication Engineering
Course Code: ECT 736	Course Name: Medical Engineering & Systems
Credit:3	L-T-P:3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 12/13/14 weeks excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components;

(i) Weekly Submissions (Internal assessment)	30%
(ii) Mid-term examinations	30%
(iii) End Semester Examination	40%

Course contents:

Module 1: Physiological Signal Processing

Physiology: Basics of ECG Signal and its Acquisition, Electrical activity of heart, ECG Waveform, Interpretation of ECG, Introduction of EEG Signal, EEG Acquisition, Neural activity in the brain, Signal Propagation in the brain, EMG signal, EMG recording, Signal processing and Filtering of EEG, ECG, EMG etc. **[8 Hours]**

Module 2: Wearable Device and Healthcare Technologies

Health monitoring with wearable sensors, Wearable electrodes of ECG, EEG & EMG, Accelerometer, Glucose sensing device, Smart healthcare components- cHealth, eHealth and mHealth. Role of IoT in Healthcare, Electronics Health Records, Concept of Bioinformatics, Security and Privacy of Health records **[8 Hours]**

Module 3: Machine Learning for Health information

Data & Modelling of Health information, Basics concepts of ML, Role of ML for Healthcare, Feature Extraction of real-world signals as speech, audio, text, image, video., Pre-processing Requirements of signals, Noise and artifacts, information retrieval, Optimization, Regression, Classification, Unsupervised Learning for Health data, Pattern Recognition, Gaussian models, Time series modelling. **[10 Hours]**

Module 4: Deep learning for healthcare

Basics of DL, MLP, Back Prorogation, Convolutional Neural Networks & Recurrent Neural network for digital health, Forward and Backward propagations, Architectures for sequence to sequence and sequence to vector mapping, Models for Healthcare using deep, recurrent and deep networks, LSTM, Medical Image analysis, Need for Deep Learning & Neuroimaging, Object Detection, Segmentation, Deep learning models. **[8 Hours]**

Module 5: Medical Devices and Systems

Risks of Integration and Healthcare Systems Testing & Evaluation, Vitro/Vivo testing, Regulatory requirements of medical devices, Standards of medical device, quality assurance Medical Device Classification, Risk management system for medical devices, Certification of medical device, Ethical regulation of medical devices & systems, Medical Devices regulation in India, USA and other countries. **[4 Hours]**

Course Outcomes:

CO1: To understand the basic concepts of various physiological signals and their processing (Knowledge)
CO2: To understand and design the medical devices and technologies for healthcare (Cognitive, Understanding)
CO3: To learn and develop the machine learning models for healthcare applications (Affective, creative)
CO4: To aware of various risk, ethical and regulatory rules for medical devices & systems (Cognitive- Analytic)

Textbooks:

References:

1. Introduction to Biomedical Engineering by John Enderle , Joseph Bronzino Academic Press
2. Biomedical Engineering: Bridging Medicine and Technology by W. Mark Saltzman, Cambridge
3. Machine Learning and Analytics in Healthcare Systems: Principles and Applications (Green Engineering and Technology) by Himani Bansal, Balamurugan Balusamy, et al., CRC.
4. Machine Learning in Medicine by Ayman El-Baz and Jasjit S. Suri, Chapman & Hall/CRC Health Informatics,
5. Demystifying Big Data, Machine Learning, and Deep Learning for Healthcare Analytics by Pradeep N, Sandeep Kautish, et al., Academic Press

Online/E-resources:

Program: M Tech. Embedded Systems	Department: Electronics & Communication Engineering
Course Code: CPT602	Course Name: Parallel & Distributed Systems
Credit: 3	L-T-P:
Pre-requisite Course:	
Objectives: **COURSE DURATION:** 12/13/14 weeks excluding examinations **COURSE ASSESSMENT** The Course Assessment (culminating to the final grade), will be made up of the following three components; (i) Weekly Submissions (Internal assessment) 30% (ii) Mid-term examinations 30% (iii) End Semester Examination 40%	
(To be Borrowed from The Syllabus of M Tech in CSE)	

Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT761	Course Name: Special Modules in Embedded Systems – 1 (IoT)
Credit: 1	L-T-P: 1-0-0
Pre-requisite course: None	

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	40%
(ii) Mid (term) examinations/Quizzes	20%
(iii) End (Semester) Examination	40%

Course contents:

- Current advances in Embedded Systems & IoT as defined by instructor- Following is suggested but not restrictive:
- Internet of everything, industrial IoT, Industry 4.0

Course Outcomes:

CO1: To analyze & implement an IoT device with communication to cloud (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative)

Textbooks: - Books on niche areas;

References:

Current literature from quality journals & magazines such as IEEE, ACM, IET etc. & others;

Online/E-resources:

Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT762	**Course Name: Special Modules in Embedded Systems – 2 (Intelligent systems)**
Credit: 1	**L-T-P: 1-0-0**
Pre-requisite course: None	

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	40%
(ii) Mid (term) examinations/Quizzes	20%
(iii) End (Semester) Examination	40%

Course contents:

- Current advances in Embedded Systems & IoT as defined by instructor- Following is suggested but not restrictive:
  - Cyber physical systems; intelligent systems
  - Self-aware systems

Course Outcomes:

CO1: To analyze & implement CPS/intelligent systems design/structure (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative)

Textbooks: - Books on niche areas;

References:

Current literature from quality journals & magazines such as IEEE, ACM, IET etc. & others;

Online/E-resources:

Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT763	Course Name: Special Modules in Embedded Systems – 3 (Linguistics)
Credit: 1	L-T-P: 1-0-0
Pre-requisite course: None	

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	40%
(ii) Mid (term) examinations/Quizzes	00%
(iii) End (Semester) Examination	40%

Course contents:

- Current advances in Embedded Systems & IoT as defined by instructor - Following is suggested but not restrictive:
  - Computational Intelligence & Linguistics
  - Probabilistic language processing

Course outcomes:

CO1: To analyze & implement language translation techniques (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative).

Textbooks: Books on niche areas;

References:

Current literature from quality journals & magazines such as IEEE, ACM, IET etc. & others;

Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT764	**Course Name: Special Modules in Embedded Systems – 4 (Embedded SoC)**
Credit: 1	**L-T-P: 1-0-0**

Pre-requisite course: None

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	40%
(ii) Mid (term) examinations/Quizzes	20%
(iii) End (Semester) Examination	40%

Course contents: As per decision of experts/industry-person/faculty-instructor

Course Outcomes:

CO1: To analyze & implement SoC/large system design/structure (simulation/fabrication) (Skills, Evaluate)

CO2: To enable her/him to perform research problem solution in a niche & socially relevant area (Affective, creative)

Textbooks:

References:

Online/E- resources:

Program: M. Tech. Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT648A	Course Name: Hardware Description Language
Credit: 1	L-T-P: 1-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	40%
(ii) Mid (term) examinations/Quizzes	20%
(iii) End (Semester) Examination	40%

Course contents:

UNIT-I HDL Simulation and Synthesis

Synthesis and simulation using HDLs- Logic synthesis using Verilog. FSM synthesis, Continuation, Data path Synthesis, Performance driven synthesis, Types of simulation, Problem solving, Static timing analysis. Formal verification, Switch level and transistor level simulation, Problem solving, Tutorial.

UNIT-II Verilog –A and Verilog- AMS

Analog/Mixed Signal Modeling and Verification-Introduction, Analog/Mixed signal modelling using Verilog-A, Analog/Mixed signal modelling using Verilog-AMS, Event Driven Modelling: Real number modelling of Analog/Mixed blocks modelling;

Course Outcomes:

At the end of the course the student will be able to:

CO1: Design capture, writing synthesizable Verilog and VHDL code.
CO2: Application of Verilog in digital system

Textbooks:

References:

1. S. Sutherland, S. Davidmann, P. Flake, "System Verilog for Design (2/e)" Springer,2006.
2. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2008.
3. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
4. Recent literature in Electronic Design Automation Tools.
5. Z. Dr Mark, "Digital System Design with SystemVerilog", Pearson 2010;

Program: M. Tech. Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT648B	Course Name: Language/s for Simulation/Verification
Credit: 3	L-T-P: 3-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	40%
(ii) Mid (term) examinations/quizzes	20%
(iii) End (Semester) Examination	40%

Course contents: Combined syllabus of ECT648A, 648B and 648C

UNIT-I VLSI Design Verification (Selected Topics)

System Verilog- Introduction- Design hierarchy, Data types, Operators and language constructs, Functional coverage, Assertions, Interfaces and test bench structures, Assertions, Interfaces and test bench structures, OVM, UVM. Discussions.

UNIT-II Verilog –A and Verilog- AMS

Analog/Digital Boundary Issues: boundary issues coverage

Course Outcomes:

At the end of the course the student will be able to:

CO1: Application of system Verilog in digital system & verification

CO2: Model Analog and Mixed signal blocks using Verilog A and Verilog AMS

Textbooks:

References:

1. S. Sutherland, S. Davidmann, P. Flake, "System Verilog for Design (2/e)" Springer, 2006.
2. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2008.
3. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
4. Recent literature in Electronic Design Automation Tools.
5. Z. Dr Mark, "Digital System Design with SystemVerilog", Pearson 2010;

Program: *M. Tech. (Embedded Systems)*	Department: *Electronics & Comm. Engg.*
Course Code: ECT741	**Course Name: Quantum Computing**
Credit: 3	**L-T-P: 3-0-0**
Pre-requisite course:	

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	30%
(ii) Mid (term) examinations/quizzes	40%
(iii) End (Semester) Examination	40%

Course contents:

UNIT I

Introduction to Quantum Computing, History, State of the Art, Quantum Bits, Quantum algorithms, Quantum Information with experimental results, Linear Algebra: basis, linear independence, matrices, Pauli matrices, Inner products, Eigenvalues, Eigenvectors, Adjoints, Hermitian operators, Tensor products, Commutator, anti-Commutator, Singular Value Decompositions

UNIT II

Postulates of Quantum Mechanics (QM): State Space, Evolution, Quantum measurements, Postulates of QM: Quantum states, projective measurements, POVM measurements, Postulates of QM: Phase, Composite systems, Density operator, Ensembles of quantum states, Properties of density operator, Schmidt Decomposition and purifications, EPR and Bell inequality, Models of computation, Analysis of computational problem, Computer science perspectives

UNIT III

Quantum Algorithms, Single Qubit operations, Controlled operations, Measurement, Universal quantum gates, A discrete set of universal operations, quantum circuit model of computation, Simulation of quantum systems, The quantum Fourier transform, Phase estimation, General applications of the quantum Fourier transform

UNIT IV

The quantum search algorithm, Quantum search as a quantum simulation, Quantum counting, Speeding up the solution of NP-complete problems, Quantum search of an unstructured database, Optimality of the search algorithm, Algorithm Limits, Quantum computers: physical realization, Guiding principles, Conditions for quantum computation, Quantum computers: implementation schemes

UNIT V

Classical noise and Markov processes, Quantum operations, Quantum noise and quantum operations, Applications of quantum operations, Limitations of the quantum operations formalism, Distance measures for classical information, Trace distance, fidelity, Quantum channel

Course-Outcomes:

At the end of the course students should be able to:

CO1: Understand the main ideas in the area of quantum computing.
CO2: Understand the basic postulates of quantum mechanics.
CO3: Apply the quantum gates to perform quantum operations.
CO4: Understand the challenges in implementing quantum algorithms.
CO5: Represent the quantum information and communicating it using quantum states.

Textbooks:

1. Nielsen M. A., Quantum Computation and Quantum Information, Cambridge University Press.
2. Benenti G., Casati G. and Strini G., Principles of Quantum Computation and Information, Vol. I: Basic Concepts, Vol II: Basic Tools and Special Topics, World Scientific.
3. Pittenger A. O., An Introduction to Quantum Computing Algorithms

Reference

Online/E-resources:

Program: M. Tech. Embedded Systems	Department: Electronics & Communication Engineering
Course Code: ECT648C	Course Name: Scripting Language
Credit: 1	L-T-P: 1-0-0
Pre-requisite Course:	

Objectives:

COURSE DURATION: 1-week intense/4-week intense/whole-semester excluding examinations

COURSE ASSESSMENT

The Course Assessment (culminating to the final grade), will be made up of the following three components; depending upon expert engaging & duration of engagement (1-week intense or 1-month or whole semester)

(i) CWS/problem-solving (Internal assessment)	40%
(ii) Mid (term) examinations/Quizzes	20%
(iii) End (Semester) Examination	40%

Course contents: Combined syllabus of ECT648A, 648B and 648C

UNIT-I UNIX and SCRIPTING

Introduction to UNIX commands, Handling directories, Filters and Piping, Wildcards and Regular expression, Power Filters and Files Redirection, Working on Vi/Vim/gvim editor, Basic Shell Programming, TCL, Perl and Python Scripting language.

UNIT II Advances in Scripting and System design

New softwares/languages recently used in industry. Case studies.

Course Outcomes:

At the end of the course the student will be able to:

CO1: execute the special features of VLSI back end and front end CAD tools and UNIX shell script
CO2: Understand the new scripting languages,system design softwares and EDA tools.

Textbooks:

References:

1. S. Sutherland, S. Davidmann, P. Flake, "System Verilog for Design (2/e)" Springer,2006.
2. M.J.S. Smith, "Application Specific Integrated Circuits", Pearson, 2008.
3. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley 1999.
4. Recent literature in Electronic Design Automation Tools.
5. Z. Dr Mark, "Digital System Design with SystemVerilog", Pearson 2010;